

An All-Solid-State Broad-Band Frequency Multiplier Chain at 1500 GHz

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Abstract—We report the results of a high-performance all-solid-state broad-band frequency multiplier chain at 1500 GHz, which uses four cascaded planar Schottky-barrier varactor doublers. The multipliers are driven by monolithic-microwave integrated-circuit-based high electron-mobility transistor power amplifiers around 95 GHz with 100–150 mW of pump power. The design incorporates balanced doublers utilizing novel *substrateless* and *membrane* device fabrication technologies, achieving low-loss broad-band multipliers working in the terahertz range. For a drive power of approximately 100 mW in the 88–99-GHz range, the doublers achieved room-temperature peak efficiencies of approximately 30% at the 190-GHz stage, 20% at 375 GHz, 9% at 750 GHz, and 4% at the 1500-GHz stage. When the chain was cooled to 120 K, approximately 40 μ W of peak output power was measured for 100 mW of input pump power.

Index Terms—Balanced doubler, broad-band solid-state multipliers, Schottky-barrier diode.

I. INTRODUCTION

TRADITIONALLY, frequency sources at submillimeter wavelengths typically consisted of cascaded whisker-contacted Schottky diode frequency multipliers driven by phased-locked Gunn oscillators [1]–[3]. Frequency tuning was achieved with mechanical tuners, and multipliers were mechanically fragile. At frequencies approximately above 1 THz, the available power was too low to drive a mixer and, thus, compact solid-state sources gave way to massive far infrared (FIR) lasers, where changing frequencies implies changing the gas in the laser, and frequencies produced must be chosen from a finite list of available laser lines. However, tremendous progress has been made in the field of solid-state frequency multipliers in the terahertz regime over the last couple of years [4]–[7]. The major push in the technology advancement in this field is primarily driven by space-borne and ground-based astronomical instruments, such as the Herschel Space Observatory (HSO) [8] and Atacama large millimeter array (ALMA) [9]. The main factors contributing to this unprecedented advancement, both in terms of efficiency/output power and higher frequency operations, can be attributed to a few different areas. Monolithic microwave integrated circuit (MMIC) power amplifiers with impressive gain in the *Ka*- to *W*-band [10] have enabled the use of microwave synthesizers that can be actively multiplied to

provide a high-power frequency-agile source beyond 100 GHz. Breakthroughs in device fabrication techniques, specifically the usage of gallium-arsenide (GaAs)-based *substrateless* and *membrane* technologies [11] along with metal beamleads for coupling probes and RF/dc ground contacts have made low-loss planar Schottky varactor diode design at terahertz frequencies feasible. Improvement of electromagnetic and nonlinear computational tools such as Ansoft's *High Frequency Structure Simulator (HFSS)*¹ and Agilent Technologies' *Advanced Design System (ADS)*², and advanced device modeling techniques in the terahertz range [12]–[15] have made design iterations faster and accurate. Finally, new circuit topologies, such as removing the dielectric substrate underneath the metal traces at specific locations to minimize dielectric loading and reduction of circuit loss, integrated silicon-nitride capacitors with other circuit elements, and balanced multiplier design techniques [16] have made integrated and compact designs made possible. Progress has also been made in single barrier varactor (SBV) and heterostructure barrier varactor (HBV) frequency multipliers [17], [18] and quantum-cascade lasers [19]. However, HBVs have shown good efficiency at frequencies well below 1 THz [20], and the most recent quantum-cascade lasers work at frequencies above 3 THz.

Heterodyne instruments at submillimeter wavelengths for ground-based and space-borne applications require broad-band fixed-tuned all-solid-state local oscillator (LO) sources, which are mechanically robust, reliable, easy to implement, and cryogenically coolable [21]. In this paper, we describe such a broad-band frequency multiplier chain at 1500 GHz for use as the LO source to drive hot electron bolometer (HEB) mixers. A similar chain could be used to pump the mixers for the heterodyne instrument for the far-infrared (HIFI) [22] of the HSO. High-resolution spectroscopic studies of the interstellar medium to observe lines such as the N^+ fine structure line at 1461 GHz, the $CO J = 15 \rightarrow 14$ rotational transition at 1611.79 GHz, and a few other lines at these frequencies—mostly from water—have important astronomical significance.

The 1500-GHz frequency chain, covering the 1408–1584-GHz band, was implemented using four cascaded planar Schottky-barrier varactor diode frequency doublers driven by a source in the 88–99-GHz range. The input drive frequency was first amplified with a MMIC power-amplifier module [10], which has a typical gain of 20 dB and consumes approximately

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²*Advanced Design System, Ver. 2.0*, Agilent Technol., Palo Alto, CA.

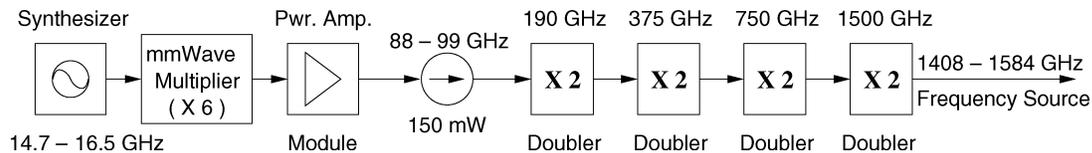


Fig. 1. Schematic block diagram of the all-solid-state 1500-GHz multiplier source using a cascade of four frequency doublers.

6 W of dc power, to generate pump power in the 100–150-mW range. All four of the doublers in the multiplier chain use a balanced planar diode configuration, incorporating symmetrical series of diodes configured in such a way that they only respond to odd harmonics at the input and even harmonics at the output. This greatly enhances separation of the input and output signal frequencies. This not only simplifies the circuits, but also enables broad-band operation since almost no additional frequency filtering is required within the impedance matching circuitry. A schematic block diagram of the multiplier chain is shown in Fig. 1. The aim in this endeavor was to generate at least $2 \mu\text{W}$ of power in the 1408–1584-GHz range to adequately pump HEB mixers [23]. It was also kept in mind that if sufficiently more power could be generated (more than $10 \mu\text{W}$), then future superconductor–insulator–superconductor (SIS) mixers [24] and multipixel heterodyne array instruments operating at these frequencies could also be driven by this source.

II. FREQUENCY-MULTIPLIER DESIGN

The multipliers are designed using a three-step process. A nonlinear harmonic-balance simulator and a Schottky varactor diode model implementation developed at the Jet Propulsion Laboratory (JPL), Pasadena, CA [12], are used to optimize the doping profile and diode dimensions such as the anode and mesa sizes and the number of diodes to be used in the circuit for a given input pump power. This calculation also determines the diode junction characteristics as a function of frequency and the embedding impedances required for optimum performance of the multipliers. The multiplier input and output circuits are synthesized using *HFSS*, a finite-element electromagnetic simulator, to calculate their *S*-parameters in an iterative procedure. To simplify and speed up the process, the passive circuitry is divided into individual elements giving several *S*-parameter matrices. They are then entered into a linear simulator along with the diode impedances obtained from the nonlinear simulator. Most of the impedance matching is accomplished using waveguide and stripline sections, which can be accurately represented in the linear simulator, simplifying their optimization. Moreover, much use is made of the symmetries of the balanced design to further speed up the design. Finally, the diode nonlinear models and the *S*-parameter matrices of the complete passive circuits obtained from *HFSS* simulations are recombined in the nonlinear harmonic balance simulator to determine the overall performance.

All the multipliers in the chain are designed with split waveguide blocks where the diodes sit in the reduced-height input waveguide. The multipliers were designed for room-temperature operations, however, they were cryogenically cooled and tested at 120 K. Fig. 2 shows the sketch of one of the typical doubler chips placed inside the split block. The input signal

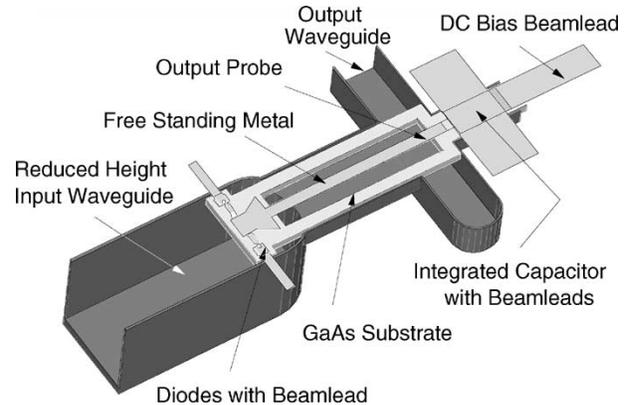


Fig. 2. Sketch of a doubler similar to the third-stage multiplier of the 1500-GHz chain. The multiplier chip rests on its beamleads on the split waveguide block. The diodes, which mostly operate in the reverse bias condition, are biased through the bias beamlead.

is directly coupled to the diodes through several sections of matching waveguides. The output signal is coupled to the output reduced-height waveguide through an *E*-field probe. The input backshort is optimized along with the input waveguide tuning sections to couple maximum power to the diodes. The output signal travels through an optimized waveguide channel in the TEM mode. The circuit symmetry prevents the input frequency from leaking into the output and the output signal from leaking into the input, as long as the reduced-height input guide is cut off for the TM_{11} mode. The output circuit is optimized using waveguide-matching components, including a backshort and a short section of metal line near the diodes acting as an open stub. This helps cancel the excess inductance of the diode structure at the output frequency. An integrated silicon–nitride capacitor at the end of the output coupling probe is used as an RF short and dc bypass. A bias beamlead connects the integrated capacitor to an external chip capacitor as an insulated standoff. The first-stage doubler is dispensed with the integrated capacitor and uses the chip capacitor alone. It is important to pay close attention to the block area holding the integrated capacitor, ensuring no leakage of RF power through that section. The diodes are grounded to the waveguide block with the two beamleads, as shown on the left-hand side in Fig. 2.

The first two doublers of the multiplier chain are driven by relatively high RF power, and thermal issues must be factored into the design. Heat generated in the anode area is propagated out to the multiplier blocks through the GaAs substrate and gold beamleads. Therefore, the thickness of the GaAs substrate is an important design issue and, hence, the first three stages of the multiplier chain, which use the substrateless technique, are designed on 40-, 22-, and 12- μm -thick GaAs substrates, respectively. The last stage of the multiplier chain, where heat is not an issue, is known as the membrane design since it is designed on a 3- μm -thick GaAs membrane.

The optimum input pump power for the first-stage doubler was determined taking various issues into consideration, such as the available output power from the power-amplifier module, the breakdown voltage of the devices, the expected efficiency of the doubler, and the required power at the output of the 1500-GHz final-stage doubler. The optimum drive power for the subsequent stages were calculated from the expected output power from the first-stage doubler and the calculated efficiency of the other three multiplier stages.

A. Substrateless Design

The first three stages of the multiplier chain are designed using what we call the substrateless design technique. To reduce RF losses in the metal lines fabricated on the GaAs substrate and to minimize dielectric loading of the waveguide, we utilize this design methodology for multipliers working approximately up to 1 THz. This technology relies on standard processing techniques to fabricate the diode structures and metal lines on the front side of the wafer. During backside processing the wafer is patterned and etched to remove GaAs from under most of the transmission-line metal, leaving freestanding metal lines suspended in air from a GaAs frame, as shown in Fig. 2. The Schottky diodes sit on one edge of this frame, resulting in a substrateless structure monolithically incorporating both the active devices and the close-in metallic circuitry. There are several advantages to the substrateless technology. Without the semiconductor underneath the lines, a wider line is required to give a specific impedance so both conductive and dielectric losses are reduced. Lack of dielectric helps prevent multimoding, which would otherwise be exacerbated by the presence of GaAs. This permits a much more flexible design procedure, and also results in physically larger diode chips, allowing easier handling and mounting, while at the same time enabling the diodes to be precisely aligned with the most critical circuitry.

The first-stage 190-GHz doubler uses a six-diode array, three on each arm, in a balanced configuration. The diodes use an epitaxial layer doping of $2 \times 10^{17} \text{ cm}^{-3}$ and diode anode size of $10.8 \mu\text{m} \times 3.5 \mu\text{m}$. Our diode model calculations predicts a zero-bias junction capacitance of 58 fF and a series resistance of 3Ω for these devices. This doubler was optimized for input pump power in the vicinity of 150 mW.

The 375-GHz second-stage doubler was designed using an array of four diodes, two on each arm. These diodes use an epitaxial layer doping of $2 \times 10^{17} \text{ cm}^{-3}$ and diode anode size of $3.6 \mu\text{m} \times 1.5 \mu\text{m}$, giving a calculated zero-bias junction capacitance of 8.9 fF and a series resistance of 15Ω . This design was optimized for 40 mW of input pump power.

The third-stage doubler (750 GHz) uses one diode in each arm, totaling an array of two diodes, with $2 \times 10^{17} \text{ cm}^{-3}$ epitaxial layer doping. The anode size of $1.5 \mu\text{m} \times 1.0 \mu\text{m}$ resulted in a calculated zero-bias junction capacitance of 2.6 fF and a series resistance of 50Ω . This doubler was optimized to operate with 7 mW of input pump power.

B. Membrane Design

The primary limitations to extend substrateless technology to frequencies beyond 1 THz are the error tolerances in positioning the diodes on the frame, and the frame itself, which lies

TABLE I
SUMMARY OF MULTIPLIER DEVICES

Doubler	Doping $\times 10^{17} \text{ cm}^{-3}$	Anode Size ($\mu\text{m} \times \mu\text{m}$)	No. of Diodes	Calculated	
				C_{j0}	R_s
190 GHz	2	10.8×3.5	6	58fF	3Ω
375 GHz	2	3.6×1.5	4	8.9fF	15Ω
750 GHz	2	1.5×1.0	2	2.6fF	50Ω
1500 GHz	5	0.8×0.2	2	0.5fF	200Ω

in the output matching waveguide. Simulations have shown that having the frame in the output waveguide does not substantially effect either the propagation in the guide or the coupling from diodes to the guide. However, the dimensions of the output circuitry and frame must be carefully tailored to prevent waveguide modes other than the TEM mode from leaking between the diodes and output guide. This would adversely affect the performance of the output circuit. To mitigate the problem, for the 1500-GHz doubler, we used what is known as membrane design technology, where the devices are fabricated on a $3\text{-}\mu\text{m}$ GaAs membrane. Unlike the substrateless design, in this design, the GaAs substrate is not removed from underneath the metallic transmission lines since the membrane is only $3\text{-}\mu\text{m}$ thick. Overall design philosophy for the membrane design is similar to the substrateless design, except for the circuit topology, which needs to be consistent with the membrane fabrication process steps, described in Section III-B.

Unlike the first three stages of the doublers, which mostly operate in a pure varactor mode, the 1500-GHz doubler operates in a hybrid mode, although more in the varistor mode than the varactor mode, resulting in a lower doubler efficiency compared to the first three stages. Since the junction area for the diodes are small and the doubler is under-pumped due to a lack of adequate pump power, the nonlinear capacitance of the diodes could not be optimally modulated. Additionally, the optimal bias condition for these devices were found to be zero bias or marginally forward biased, modulating the nonlinear resistance of the diodes. This resulted in the devices to operate in a hybrid varactor-varistor mode. This doubler was designed with two diodes, one on each arm. The diodes use an epitaxial layer doping of $5 \times 10^{17} \text{ cm}^{-3}$ and diode anode size of $0.8 \mu\text{m} \times 0.2 \mu\text{m}$, resulting in a calculated zero-bias junction capacitance of 0.5 fF and a series resistance of 200Ω . Higher epitaxial layer doping results in a lower series resistance and higher multiplier efficiency for the devices. In this design, the diodes were put in the input waveguide, unlike the design by Erickson *et al.* [25], where the diodes were in the output waveguide. The design was optimized for $500 \mu\text{W}$ of input pump power. However, simulations show that drive power in excess of 2 mW can safely be used. Table I shows a summary of all the device parameters for all the doublers used in the chain.

III. DEVICE FABRICATION

Fabrication of the planar Schottky-barrier varactor diode multiplier devices has been discussed in detail by Martin *et al.* [11]. Here, we will elaborate on the fabrication aspects specific to the frequency multipliers described in this paper. There are two distinct processes used for fabricating the devices for

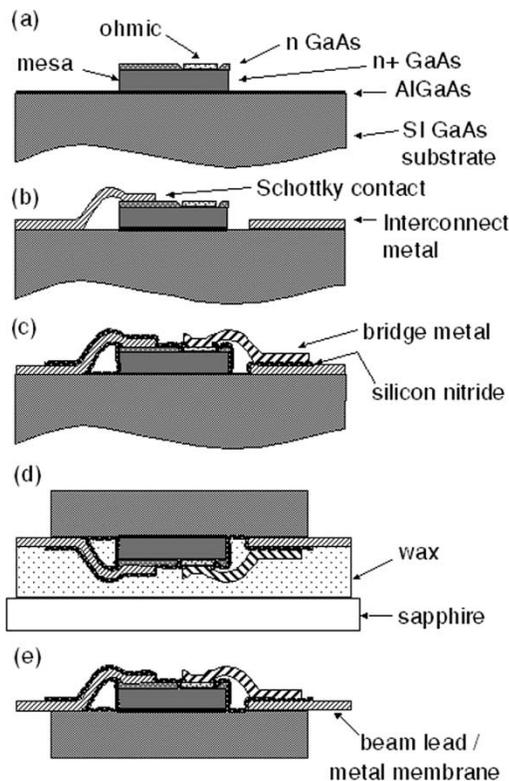


Fig. 3. Substrateless device fabrication process steps. (a) Ohmic and mesa definition. (b) Interconnect metal and air-bridged Schottky deposition. (c) Passivation and bridge metal definition. (d) Backside thinning and device separation. (e) Release of device from carrier wafer.

the 1500-GHz multiplier chain. For the devices working at frequencies below 1 THz, substrateless technology [26] with optical lithography and conventional epitaxial layer designs was used. For devices operating beyond 1 THz, electron-beam lithography with complex epitaxial layers to allow GaAs membrane definition was used. The two process steps used to fabricate the devices for the chain are described separately below.

A. Substrateless Process

Fig. 3 shows the different steps used for the substrateless device fabrication process. The starting material for this process is semi-insulating GaAs with epitaxial layers grown by molecular-beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD). The diode structure consists of a $\sim 200\text{-nm}$ -thick $2 \times 10^{17} \text{ cm}^{-3}$ doped n-type Schottky layer on top of a heavily doped ($5 \times 10^{18} \text{ cm}^{-3}$) $\sim 1.5\text{-}\mu\text{m}$ -thick n+ contact layer grown on a 50-nm aluminum–gallium–arsenide (AlGaAs) etch-stop layer. In the first step, the device mesas were defined using a selective dry etch, which stops at the AlGaAs etch-stop layer. An air-bridge process was then used to define the anode and interconnect metal. Following Schottky metallization and liftoff, silicon nitride (Si_3N_4) was deposited. Silicon nitride acts as the dielectric for the integrated bias capacitor in addition to passivating the diodes. The top contacts to the capacitors and the connection to the on-mesa ohmic metal area was achieved using an air-bridge metal step. The wafer was then mounted topside down onto a carrier wafer using wax. The

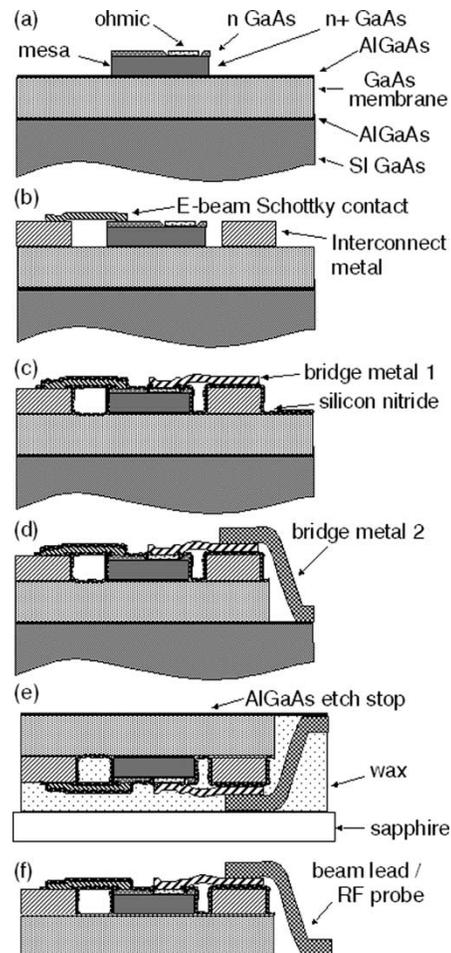


Fig. 4. Membrane device fabrication process steps. (a) Ohmic and mesa definition. (b) Interconnect metal and e-beam defined Schottky deposition. (c) Passivation and bridge metal 1 definition. (d) Membrane layer etch and bridge metal 2 deposition. (e) Removal of substrate with selective etch. (f) Release of the device from the carrier wafer.

GaAs substrate was thinned to the desired thickness ($40 \mu\text{m}$ for the 190-GHz doubler, $22 \mu\text{m}$ for the 375-GHz doubler, and $12 \mu\text{m}$ for the 750-GHz doubler) by lapping, polishing, and wet etching. The substrate was then patterned and etched by reactive ion etching (RIE)—removing the GaAs substrate from beneath some of the interconnect metal connections. This also formed the metal membrane probes and beamleads. Finally, the circuits were removed from the carrier wafer by dissolving the mounting wax.

B. Membrane Process

Wafers used for the membrane process had an additional epitaxial layer consisting of a $3\text{-}\mu\text{m}$ -thick undoped GaAs membrane layer supporting the diode layers and a 400-nm-thick second AlGaAs etch-stop layer. Doping used in this case for the 200-nm-thick n-type Schottky layer was $5 \times 10^{17} \text{ cm}^{-3}$. The ohmic contacts and mesas were defined in the same way as for the substrateless process, however, the interconnect metal and anode metals were deposited in two separate steps. The interconnect metal was deposited to a thickness equal to the height of the mesas. After defining the membrane areas of the circuit from the top side of the wafer, RIE was used to remove

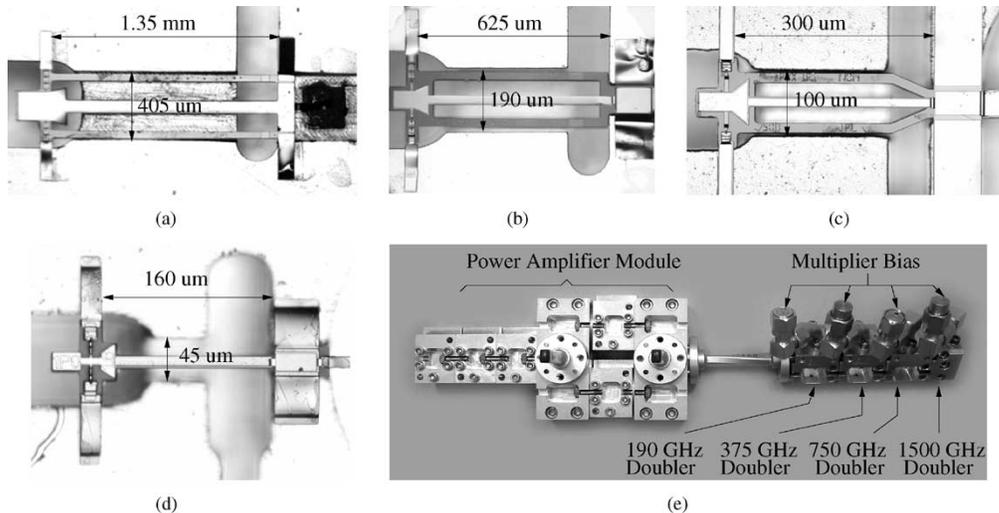


Fig. 5. Assembled doublers in the split-waveguide block with the top half of the block removed. (a) 190-GHz doubler. (b) 375-GHz doubler. (c) 750-GHz doubler. (d) 1500-GHz doubler. (e) All the doublers put together along with the MMIC power-amplifier module. The isolator and directional coupler, which are connected between the amplifier and first stage multiplier, is not shown in (e).

the silicon nitride layer, followed by another RIE of the 3- μm GaAs membrane layer, down to the second AlGaAs etch-stop layer. In the final front-side metallization step, air-bridge and beamlead metals, which are used for bias connections, mechanical support, RF tuning, and antenna probes, were deposited. The wafers were then wax mounted to a carrier wafer. The steps followed after this were similar to the substrateless process, except for an additional nonselective etch to remove the AlGaAs etch-stop layer. Fig. 4 shows the steps followed in the membrane processing.

IV. ASSEMBLY AND MEASUREMENT SETUP

Assembly of the substrateless and membrane devices are similar; however, one has to be more careful handling the membrane devices, as they are smaller. Assembly of the doublers is relatively simple. The diode chip is dropped inside the split waveguide block with the diode beamleads resting on the waveguide metal. The beamlead from the integrated silicon-nitride capacitor is bonded to an external chip capacitor, which, in turn, is wire bonded to the bias connector. There is no soldering or other high-temperature procedures used on the devices, which reduce the possibility of device damage. Photographs of assembled doublers are shown in Fig. 5. Fig. 5(a)–(d) shows the four doublers on the split-waveguide blocks with the top-halves of the blocks removed. Fig. 5(e) shows a photograph of all four of the doubler blocks put together along with the MMIC power-amplifier module.

The multiplier chain was put inside a cryostat, and its performance measured both at room and cryogenic temperatures. The thermal conductance from the multiplier chain to the mechanical cooler's cold head was chosen such that the temperature could be actively regulated by a heater controlled by a feedback loop monitoring a temperature sensor mounted on one of the multipliers. Measurements were carried out using an Erickson

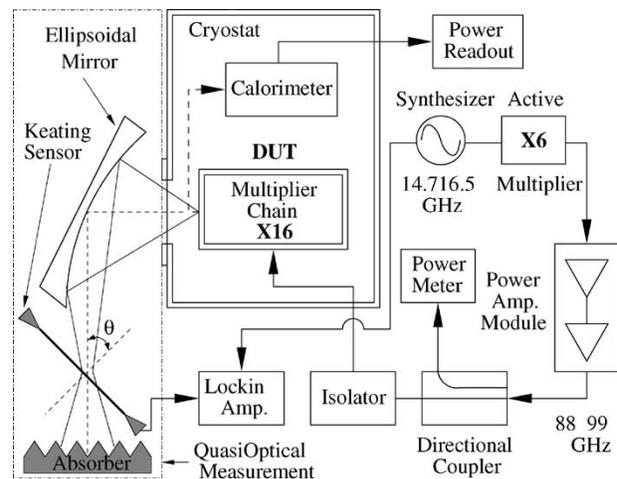


Fig. 6. Schematic of the measurement setup used to measure the multiplier chain both at room and cryogenic temperatures. The angle θ is set at Brewster angle for optimal coupling to the Keating sensor. For room-temperature measurements, the calorimeter is connected to the output of the last-stage multiplier through a waveguide transition. For measurements at cryogenic temperatures, output from the multiplier diagonal horn is measured with the Keating meter using the quasi-optical measurement setup.

calorimeter [27] and a Keating power meter,³ and both of them gave similar power readings for a given multiplier output. Fig. 6 shows a schematic diagram of the setup used for measuring the multiplier chain. An Agilent⁴ synthesizer and an active multiplier chain with a W -band head provides a few milliwatts of RF power. A power-amplifier module amplifies the input power to the appropriate drive level. The input power to the chain is monitored using a directional coupler. A low-loss broad-band isolator is used between the directional coupler and first stage doubler to avoid any load pulling.

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⁴Test and Measurement Organization, Agilent Technol., Palo Alto, CA.

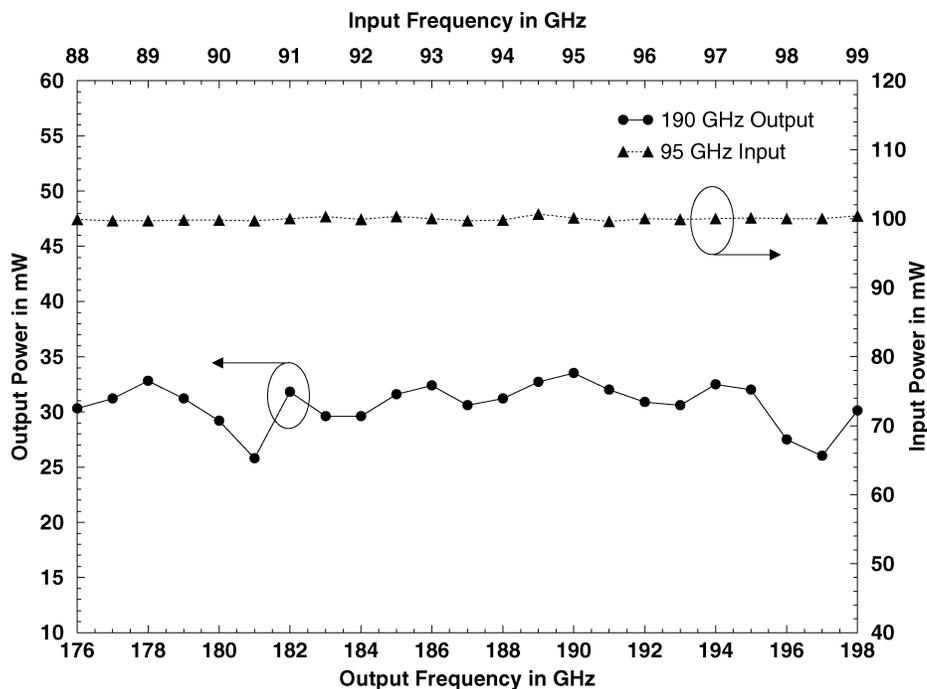


Fig. 7. Room-temperature performance of the 190-GHz doubler. The circles with the solid line is for the output power, and the triangles with the dotted line is for the input power. Input and output power for this doubler was measured using the calorimeter.

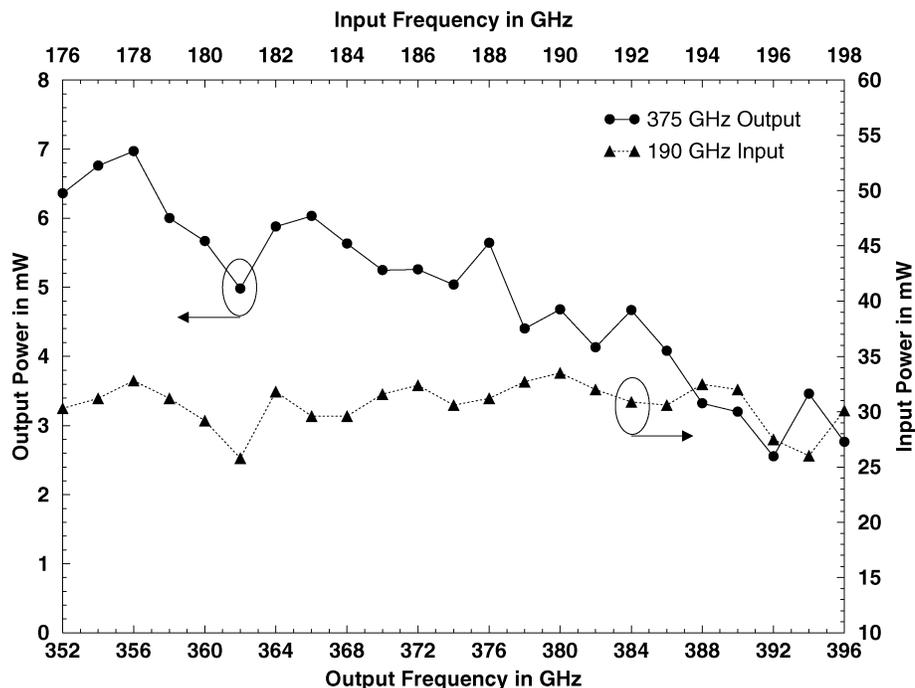


Fig. 8. Room-temperature performance of the 375-GHz doubler. The circles with the solid line is for the output power, and the triangles with the dotted line is for the input power. The input power was measured independently, not simultaneously with the output power. The calorimeter was used to measure the input and output power for this doubler.

Prior to beginning any measurements, we run a calibration at every frequency point to compute the ratio between the power at the coupled port of the directional coupler and the power where the multiplier chain is bolted in. The first three stages of the multiplier chain were measured at room temperature using the calorimeter. Appropriate tapered waveguide transitions were

used to connect the multiplier waveguide outputs to the WR-10 waveguide input of the calorimeter. The last-stage doubler has a built-in diagonal horn and was measured at room temperature with the calorimeter when the output power was more than approximately 1 μ W. However, the Keating power meter was used to measure power quasi-optically when the output power

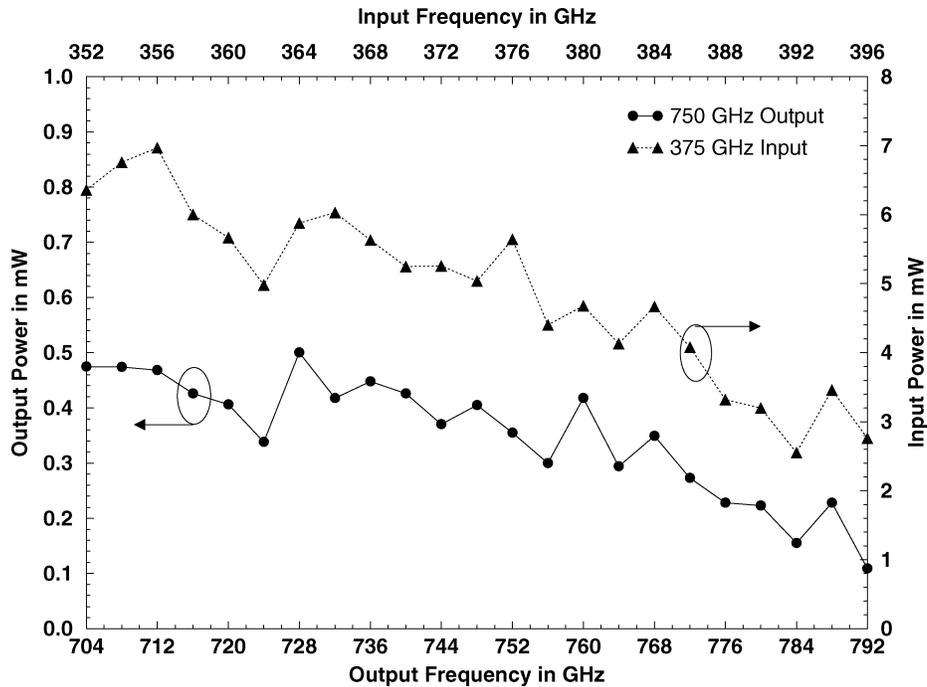


Fig. 9. Performance of the 750-GHz doubler at room temperature. The calorimeter was used to measure power from this doubler. The circles with the solid line is for the output power, and the triangles with the dotted line is for the input power. The input power was measured independently, not simultaneously with the output power.

was more than approximately $5\text{--}10\ \mu\text{W}$. Output power from the complete chain was measured at cryogenic temperatures using the Keating power meter.

For measuring power for the final stage of the 1500-GHz chain, we used a Golay⁵ cell because of its high sensitivity and fast response. However, it is very difficult to get repeatable optical coupling to the Golay cell, and the calibration is only approximate. Thus, with the Golay cell, we often did a sweep, optimizing the bias point, and later scaled the measured power based on a few points measured with the calorimeter or Keating meter. The results presented in this paper were corrected only for the window losses of the cryostat (73.5% transmission for the Mylar window); no other corrections were used for waveguide or any other losses in the measurement system.

V. RESULTS

The measured results for the first-stage 190-GHz doubler are shown in Fig. 7. The input drive power for measuring all the doublers in the chain was kept at 100 mW. Except for a few points, the output power for this multiplier was relatively flat across the band. At room temperature, we measured a peak output power of 34 mW at 190 GHz, and approximately 30 mW or more across the 176–198-GHz band.

Fig. 8 shows the results for the 375-GHz doubler, cascaded with the 190-GHz stage. The input pump power to the second doubler on the plot is shown as reference only because it was not measured simultaneously with the 375-GHz doubler output. It can be seen from Fig. 8 that the 375-GHz doubler peaked at the lower end of the band. At room temperature, the doubler

produced close to 7 mW of output power at the lower end and approximately 3 mW at the upper end of the band.

The measured results for the 750-GHz doubler, cascaded with the 190- and 375-GHz doublers, is shown in Fig. 9. Here again, the input pump power to the 750-GHz doubler is plotted for reference only, as it was not measured simultaneously with the output power. It appears from this figure that the 750-GHz doubler performance is relatively flat across the band and closely follows the input pump power. At room temperature, we measured over 0.2 mW of output power across the band for this doubler, with an approximate peak power of 0.5 mW at 730 GHz. It should also be noticed that there is hardly any ripple at the output power across the frequency band, suggesting minimal interaction and reflections between the first three stages. This is very encouraging, as we did not use any isolators between the stages.

Fig. 10 shows the measured data for the 1500-GHz doubler, cascaded with the 190-, 375-, and 750-GHz doublers. The chain was pumped with approximately 100 mW of drive power in the 88–99-GHz range, as shown in Fig. 7. Here, we have also plotted the 750-GHz doubler output power for reference only, as we measured it independently—and not while pumping the 1500-GHz doubler. It appears from the room- and cryogenic-temperature data that the bandwidth of the final stage doubler is relatively narrow compared to the other stages. At room temperature, we measured approximately $15\ \mu\text{W}$ of peak output power at 1500 GHz. When the chain was cooled to 120 K, an approximate peak output power of $40\ \mu\text{W}$ was measured at 1490 GHz. However, over most of the 1408–1584-GHz frequency band, we measured over $15\ \mu\text{W}$ of output power at 120 K. We noticed that the ripples in the output power were more pronounced when the

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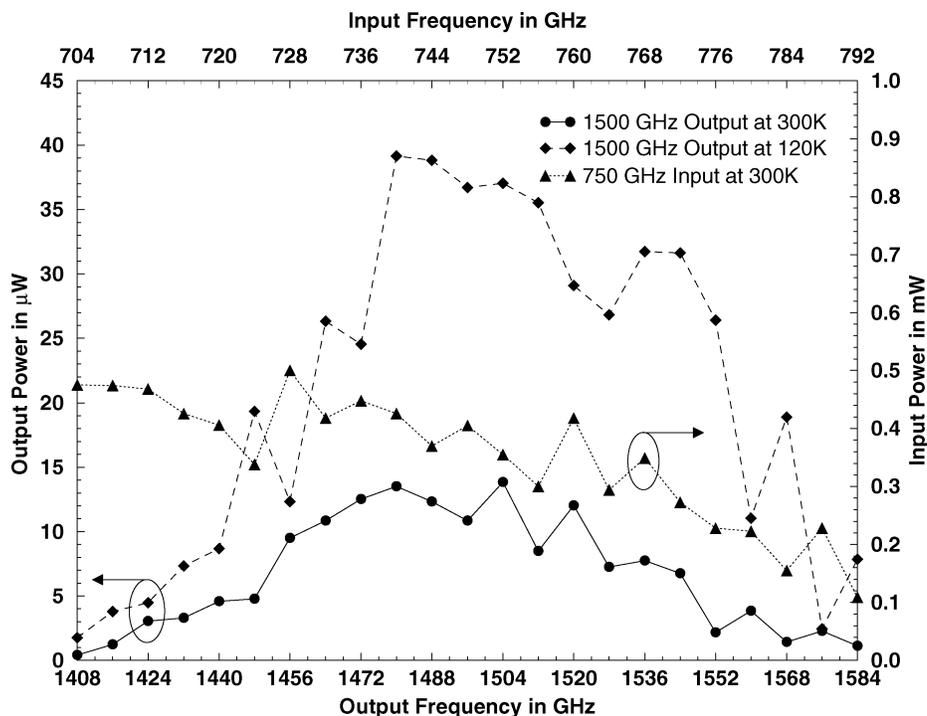


Fig. 10. Performance of the 1500-GHz chain. The circles with the solid line is for the output power at room temperature, the diamonds with the dashed line is for the output power at 120 K, and the triangles with the dotted line is for the input power. The input power was measured independently, not simultaneously with the output power.

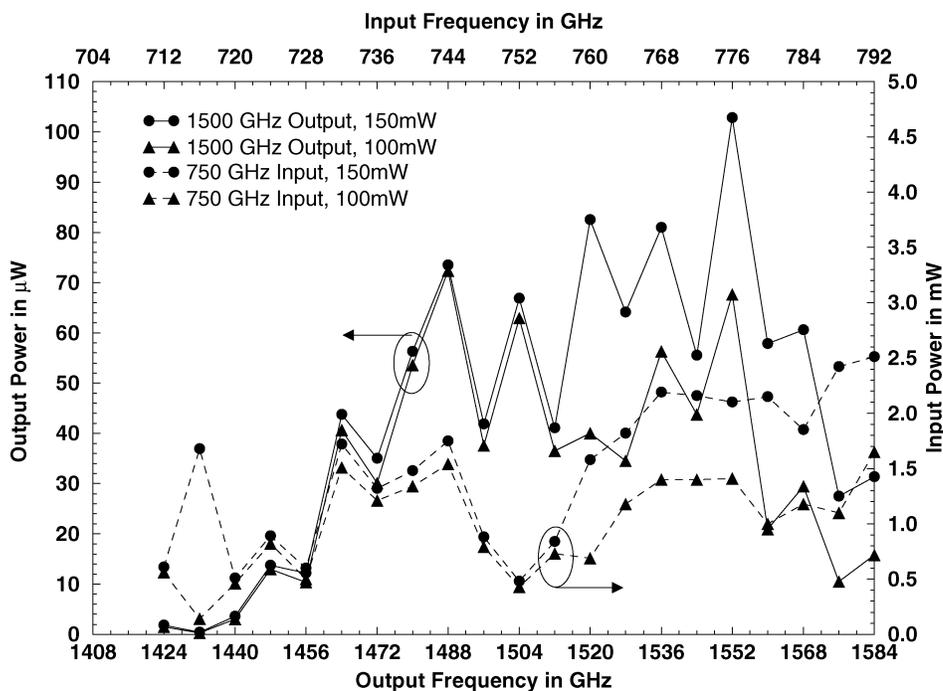


Fig. 11. Performance of another 1500-GHz chain. The circles and triangles with the solid lines are for the 1500-GHz output power at 120 K with the *W*-band drive power of 150 and 100 mW, respectively. The circles and triangles with the dashed lines are for the 750-GHz input pump power at 120 K with the *W*-band drive power of 150 and 100 mW, respectively.

chain was cooled to 120 K, suggesting stronger interaction and reflections between the stages at cryogenic temperatures com-

pared to room temperature. However, this was expected since the losses are lower at cryogenic temperatures.

A similar chain produced approximately 70- and 102- μ W peak output power at 120 K, when pumped with 100- and 150-mW input drive power in the W -band, respectively. Fig. 11 shows the performance of this chain. However, one should note that 100 mW is a safe input power level for long life and high reliability for these devices [28]. Therefore, we did not pump this chain with 150 mW of input drive power for extended operation.

VI. CONCLUSION

We have designed, built, and measured an all-solid-state broad-band complete frequency multiplier chain with four high-performance cascaded doublers. The chain produced 40 μ W of peak output power at around 1490 GHz when pumped with a 100-mW input drive signal and cooled to 120 K. Another similar chain, driven by 150 mW of an input pump signal and cooled to 120 K generated approximately 102 μ W of output power, a record high for a solid-state source at these frequencies. The new substrateless and membrane fabrication technologies with metal beamleads have made the multiplier circuits more efficient, less lossy, and easier to assemble than previous technologies. We also demonstrated that mechanically robust, electronically tunable, broad-band, light weight, and compact sources at 1500 GHz suitable for pumping heterodyne mixers for ground-based and space-borne applications can be achieved. This chain can also be used to drive future multipixel arrays of coherent detectors. This represents a major improvement in capabilities for terahertz heterodyne receivers.

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